A Manufacturing Process for Analog and Digital Gallium Arsenide Integrated Circuits

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Abstract—**A process for manufacturing small-to-medium scale GaAs integrated circuits is described. Integrated FET's, diodes, resistors, thin-film capacitors, and inductors are used for monolithic integration of digital and analog circuits. Direct implantation of Si into $>10^5$ Ω·cm resistivity substrates produces *n*-layers with ±10-percent sheet resistance variation. A planar fabrication process featuring retained anneal cap (SiO_2), proton isolation, recessed Mo–Au gates, silicon nitride passivation, and a dual-level metal system with polyimide intermetal dielectric is described. Automated on-wafer testing at frequencies up to 4 GHz is introduced, and a calculator-controlled frequency domain test system described. Circuit yields for six different circuit designs are reported, and process defect densities are inferred.**

I. Introduction

THE EARLIEST efforts at monolithic integration of gigahertz-bandwidth circuits in gallium arsenide [1] addressed the performance advantages of the technology, not the manufacturability. The subsequent application of ion implantation [2] and planar processing [3] did much to improve the GaAs integrated circuit (IC) fabrication technology. Now, as this technology moves into a more mature, applications-oriented phase, much attention is being paid to manufacturing techniques, both in fabrication and testing. This paper describes a manufacturing process for small-to-medium scale GaAs IC's of the type described in references [4]–[7] (amplifiers, counters, and RF subsystems).

The wafer fabrication portion of the process is presented, along with a description of components and process steps. Rationale is given for the incorporation of new or nonstandard process techniques. Automated on-wafer circuit testing is discussed, and a specially designed system for performing these tests at microwave frequencies is described. Finally, yield data for representative circuits fabricated and tested with this process are presented.

II. Components

The manufacturing system described here is designed to fabricate small-to-medium scale gigahertz bandwidth analog and digital GaAs IC's. The principal attributes of this high-speed process are a low-capacitance substrate and interconnection scheme (dual-layer metal), and a variety of active, as well as passive, components. The components illustrated in Fig. 1 have their key electrical parameters listed in Table I.

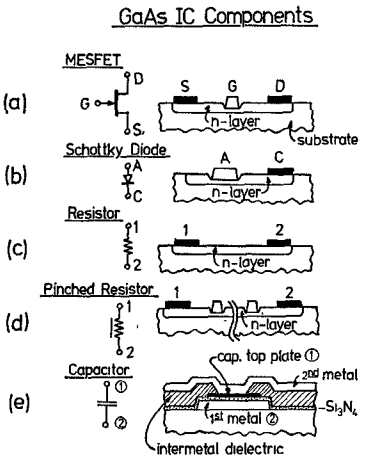

Fig. 1. Components of the GaAs IC process.

TABLE I
TYPICAL COMPONENT PARAMETERS

COMPONENT	PARAMETER	VALUE
FET	I_{DSS} (V_{DS}=3V)	200 mA/mm
	V_P (@5% I_{DSS})	-2.1 V
	g_m (V_{GS}=0V, V_{DS}=3V)	135 mS/mm
	g_m	100 mS/mm
	C_{gs} (V_{GS}=-1V, V_{DS}=3V)	1 pF/mm
	f_T	15 GHz
SCHOTTKY DIODE	$C_{JUNCTION}$	2 fF/μm²
	J_{SAT}	1.6 x 10^{-14} A/μm²
RESISTORS:		
STANDARD	R_{SHEET}	320 Ω/□
"PINCH"	R_{SHEET}	1400 Ω/□
THIN-FILM CAPACITORS	C	60,000 pF/cm²
	$V_{BREAKDOWN}$	80 V
	$I_{LEAKAGE}$ (@15 V)	1 pA
SPIRAL INDUCTORS	L	1 nH - 20 nH
	Q (10 nH@1 GHz)	1

Pinchoff voltage of the 1-μm gate-length FET is adjusted to −2.1 V by channel-thickness etching; a standard devia-

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tion of 0.31 V is maintained on a typical wafer. This pinchoff voltage choice represents a compromise between the lower pinchoff preferred for low-power digital circuits and the higher pinchoff voltage which can give lower distortion and higher output power in linear circuits. Since analog and digital circuits are often integrated together on a single chip, the use of a single-pinchoff-voltage FET tends to insure compatibility of signal amplitude between the two circuit types.

Schottky diodes, fabricated concurrently with the FET's, are used for RF detectors, switches, and level-shift elements [4], [5].

Resistors, made simply with the implanted n-layer, are used as loads and for bias adjustment, chiefly in linear circuits [7]. Where very high values of bias resistance are required, the "Pinch" resistor of Fig. 1(d) is useful, since it has over four times the average sheet resistance of the implanted resistor.

A particularly important component, and one which is not inherent to the GaAs FET process, is the thin-film metal-insulator-metal capacitor. The high capacitance per unit area (60 000 pF/cm^2) of this component makes capacitors of 1 pF to 20 pF practical, with parasitic capacitance-to-ground less than 0.1 percent. Such capacitors are especially useful for coupling and bypass applications within the chip [7].

The final component is the dual metal system itself which offers low resistance interconnects (0.37 $\Omega/\square$) and low capacitance crossovers (typ. <4 fF). Spiral inductors, though not process components in themselves, can be designed with this dual-metal system. The low observed Q values limit inductors' usefulness to peaking applications [5] in the $\leq$4-GHz frequency range typical of circuits made with this process.

III. Wafer Fabrication

The first step in GaAs IC fabrication is the formation of an n-type layer by ion implantation. For this step to be successful, and for subsequent device electrical characteristics to be satisfactory, suitable GaAs starting material must be selected. The two most basic requirements for GaAs material electrical characteristics are:

1) that bulk resistivity be sufficiently high, even after ion implant anneal, to assure acceptably low leakage currents between circuit elements;
2) that residual impurities be low enough to insure uniform and repeatable implanted-layer sheet resistance and acceptably low back-depletion layer coupling between devices ("Backgating") [8].

In early semi-insulating GaAs [9] the high-resistivity condition was often met by addition of large amounts of Cr to the crystal growth melt. This often produced material which was unacceptable for ion implantation directly into the substrate. As a result, early ion-implanted GaAs IC's [2] used low-resistivity liquid-phase epitaxially grown (LPE) "Buffer" layers [10] as the implant medium, with satisfactory results. However, cost-effective manufacturing of GaAs IC's dictates the use of direct-to-substrate ion-implantation. Suitable material is obtained by ⟨111⟩-growth of high-purity or lightly Cr-doped GaAs with the liquid-encapsulated Czochralski (LEC) method [11]. Because these ingots must be sliced along the ⟨100⟩ plane, irregularly shaped slices result. These slices are cleaved into rectangular (1.25–1.5-in) wafers for processing. The more desirable 2–3-in diameter round, ⟨100⟩-grown wafers, which are also suitable for direct-to-substrate ion implantation [12] have been evaluated, but not yet incorporated into the process described here. To assure that the high-resistivity condition is satisfied in all cases, each wafer is subjected to a nondestructive ac conductance test, and required to pass a specification equivalent to $\geq 10^5$-Ω·cm resistivity. Although material is routinely grown which far exceeds this resistivity specification, even the best ingots can exhibit conductive sections, necessitating a wafer-by-wafer screen.

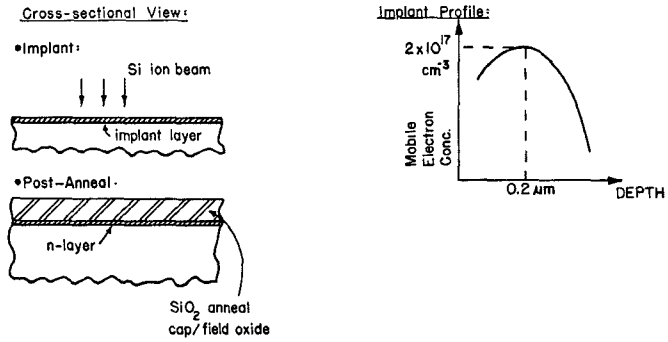


Fig. 2. Ion implantation step. Si ions are implanted at 230 keV to a dose of 6.25×10^{12}/cm^2. Mobile electron concentration is 2×10^{17}/cm^3 peak at 0.2 μm below surface.

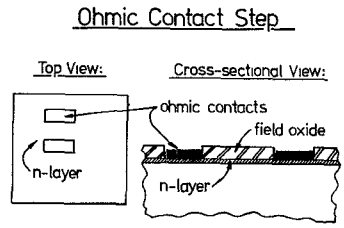


Fig. 3. Ohmic contact step. Au–Ge alloyed ohmic contacts are fabricated with the aid of field oxide lift assist.

Uncoated wafers are ion implanted with Si ions [13] at 230 keV and a dose of 6.25×10^{12}/cm^2, as shown in Fig. 2. The wafers are coated with chemical-vapor-deposited (CVD) SiO_2 420 nm thick, and annealed in H_2 ambient at 850°C for 30 min. The resulting active doping profile (Fig. 2) is 200 nm deep at the peak concentration of 2×10^{17}/cm^3. Estimated electrical activation is 75–80 percent, and nominal sheet resistance is 320 $\Omega/\square$. Sheet resistance, as measured with a contactless RF conductivity meter [14], typically varies less than ±5 percent on a given wafer. A total sheet resistance variation for all wafers has been established at ±10 percent, with high percentage of acceptance.

Standard Au–Ge alloyed ohmic contacts are produced as shown in Fig. 3. A novel feature of this process step is the use of the anneal cap, which has been retained to serve as a process-assisting field oxide. Windows are chemically

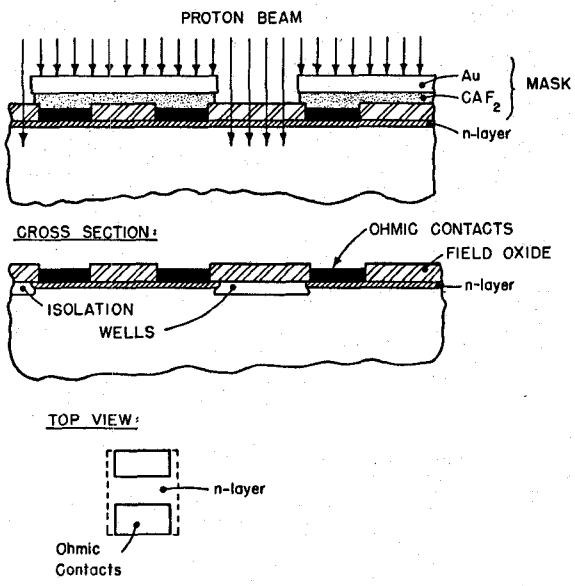


Fig. 4. Proton isolation step. Protons at 140 keV are implanted through field oxide, masked by Au-dielectric sandwich. Invisible isolation wells give superior isolation to selective implant process.

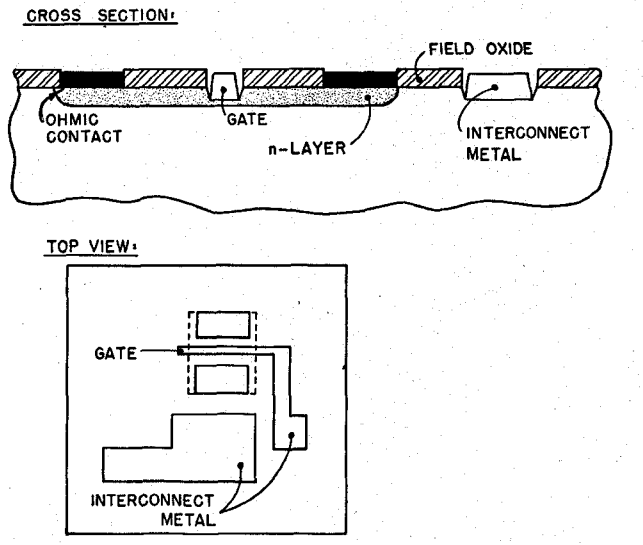


Fig. 5. Gate and first-level interconnect metal fabrication. Mo–Au gates are fabricated by contact photolithography, oxide and GaAs etching, and liftoff. Field oxide lift assist assures clean patterns.

etched in the field oxide where ohmic contacts are to appear. The undercutting of photoresist during this oxide etch produces a cantilevered photoresist overhang which insures trouble-free lifting of the deposited ohmic contact metal pattern.

The manifest advantages of planar isolation in GaAs IC fabrication have traditionally been realized with selective ion implantation [3]. The process presented here uses the slightly more complicated proton bombardment isolation, the details of which are described by D'Avanzo [8]. The principal advantages of proton isolation are:

1) improved dc leakage current isolation, especially between gate-level interconnect metal and *n*-regions, due to greatly decreased surface leakage current; and
2) reduced back-depletion layer coupling ("Backgating") between closely spaced active devices.

As shown in Fig. 4, protons are implanted through the field oxide at 140 keV with a dose of $5\times10^{14}/\text{cm}^2$. Chemical removal of the gold-dielectric mask leaves behind an essentially planar surface with proton-damaged isolation wells between devices. Leakage current between 3-μm-spaced *n*-islands is typically 10 nA at 16 V; leakage between gate-level interconnect metal and *n*-islands separated by 3 μm is 10 nA at 10 V. The "Backgating" threshold voltage is typically 7 V with undoped substrate material, effectively eliminating adjacent device backgating as a serious circuit design limitation.

The 1-μm FET gates and the first level of interconnect metal are simultaneously formed in the next process step (Fig. 5). Lithography at this step is by contact photomasking, as is the entire process. Submicrometer hard-surface masks define photoresist cuts which mask field oxide etch, gate channel etch, and metal lifting. Once again, the field oxide serves as an undercut support for overhanging photoresist, insuring a clean lift for the *E*-beam evaporated Mo–Au gate metal system. This metal system has been shown to produce Schottky barriers which are stable during subsequent (300°C) processing and accelerated device life tests. (A somewhat similar evaporated Mo–Au system proved not to be the critical lifetime-determining factor in GaAs FET reliability studies by Mizuishi *et al.* [15]).

At this point, test FET's are subjected to in-process dc and 1-MHz tests. The purpose of these tests is to reject wafers on which FET's do not meet process control specifications, thereby saving subsequent process costs. Wafers passing in-process electrical tests are next coated with a thin (100-nm) film of oxygen-free silicon nitride. This film is deposited in a parallel-plate reactor apparatus [16] at an RF power of 250 W (5 W/cm^2) onto a heated substrate (200°C). Although such films may not be stoichiometric, and contain substantial included-hydrogen, they are claimed to give increased device reliability with respect to long-term burnout, as compared to SiO_2 passivating films [17]. It has also been proposed that incorporated hydrogen in silicon nitride films plays an active role in increasing GaAs FET reliability by chemically combining with residual oxygen on the GaAs surface [17]. Plasma-enhanced CVD was chosen because:

1) it proceeds at temperatures well below the ohmic contact alloy temperature (430°C); and
2) it does not cause irreversible damage to *n*-type GaAs layers, as RF-sputtered films commonly do.

However, the high dielectric constant (6.9) of these silicon nitride films, and the tendency of thick depositions to crack, make them a poor choice for the dielectric which separates first and second metal layers, where minimum inter-layer capacitance is required.

The high dielectric constant of the silicon nitride passivation layer is exploited to make thin-film capacitors, as shown in Fig. 6. A titanium top plate is patterned by photoresist lifting over sections of first-level interconnect metal which serve as the lower capacitor plates. Nitride

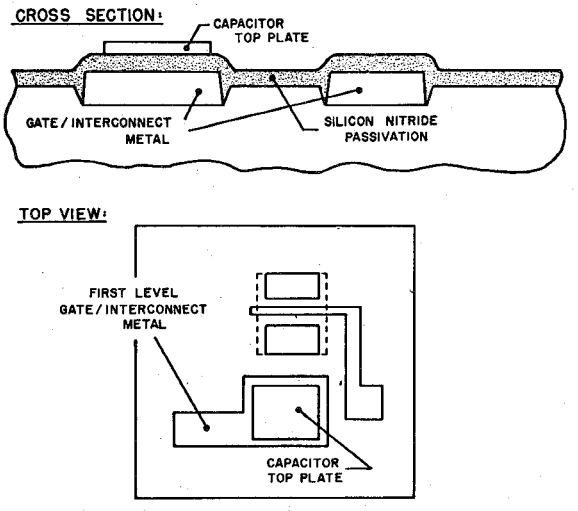


Fig. 6. Passivation and capacitor. Silicon nitride 100 nm thick is deposited by plasma CVD. Dielectric constant of 6.9 gives high (60 000 pF/cm^2) capacitance in areas where capacitor top plates are defined.

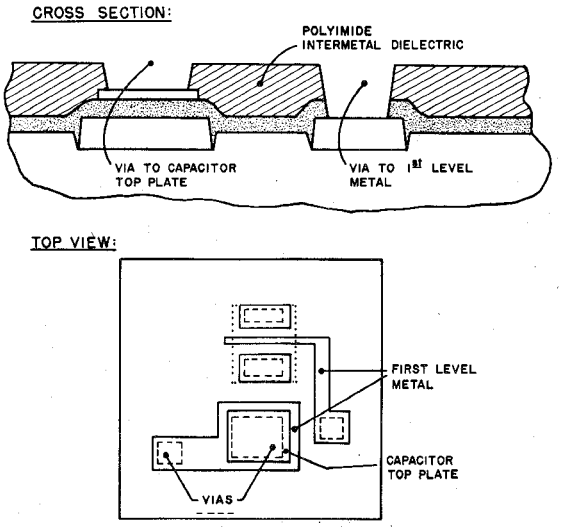


Fig. 7. Intermetal dielectric and via cut. Polyimide (Dupont PI-2555) is spun on and cured at 300°C to give smooth top surface, as shown. Vias are etched with dry ion-etch technique.

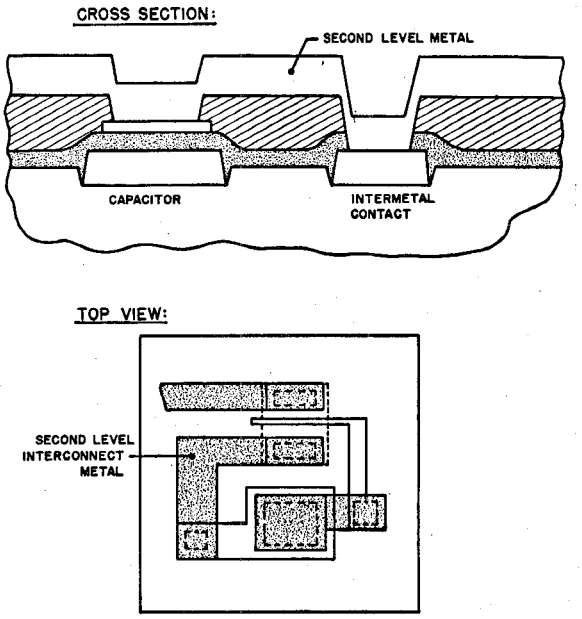


Fig. 8. Second level interconnect metal. Ti–Pt–Au metal is evaporated, then patterned with ion etching. Second metal interconnects ohmic metal, first layer metal, and capacitor top plates.

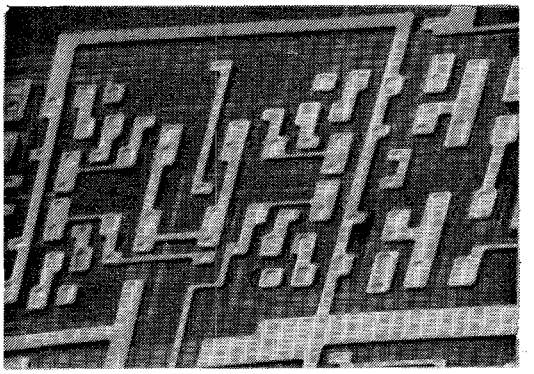


Fig. 9. Scanning electron micrograph of circuit section. First-level and second-level metal are shown, along with interconnecting vias. Wafer is later overcoated with polyimide as a scratch protector for second metal.

film quality and parameter control are such that 10-pF capacitors with active area of 1.7×10^{-4} cm^2 are produced with 90-percent yield and 5-percent standard deviation of capacitance value.

The intermetal dielectric is a spin-on polyimide film [18], [19]. This film produces an essentially flat top surface, regardless of underlying topology, and after cure at 300°C has dielectric constant, $\varepsilon_r = 3.8$, and loss tangent, $\tan\delta = 0.007$, measured at frequencies up to 2 GHz. Stress tests (15 lb/in^2 steam for 100 h, 150°C bake for 1700 h, 300°C bake for 300 h) have proven the durability of this polyimide layer. A combination of reactive ion etching (O_2 Plasma) and ion etching (Ar beam) is used to pattern "Via" openings in the polyimide and silicon nitride (Fig. 7). Where the capacitor top plate exists, it acts as an etch stop. Thus, the via openings to capacitors and first level metal are produced with one mask-and-etch operation.

Interconnection of components is accomplished with the second layer Ti–Pt–Au metal system (Fig. 8). Besides connecting first-level (gate) metal to ohmic contacts, the second metal provides low resistance (0.37 Ω/□) interconnects for high-current-carrying paths, and crossovers for signal-path wiring. Fig. 9 shows a scanning electron micrograph of the ion-etch patterned second metal on polyimide dielectric. Flatness of the polyimide over underlying features is evident.

IC fabrication is completed by coating the entire circuit with a second layer of polyimide film, whose function is to prevent handling damage to second-level metal. Bonding pads and scribe borders are opened with the via etch process.

Final wafer test consists of dc and 1-MHz audit of FET, diode, resistor, capacitor, and metallization test patterns. The purpose of these tests is wafer screening for process control. Functional testing of integrated circuits is described in the next section.

IV. Circuit Testing

Wafer testing of GaAs IC's in this manufacturing process is performed with an automated RF circuit test system (Figs. 10 and 11). There are two fundamental reasons for testing circuits this way:

1) high frequency IC's often do not function at dc or low frequencies (e.g., ac-coupled amplifiers); and
2) functional operation does not guarantee correct response over the desired range of frequencies and amplitudes.

Since rejection of chips after package assembly is expensive, an accurate on-wafer tester is essential to the economics of the process.

The high-frequency wafer test system, diagrammed in Fig. 10, consists of an RF signal source (0.01–8.4-GHz sweep signal generator), an RF detector Hz–22-GHz spectrum analyzer), dc power supplies, bias-voltage supplies, RF relays, and an automatic wafer prober. All these devices are calculator-controlled via an IEEE Std. 488 data bus. Circuit testing proceeds by applying voltages, measuring dc currents, then stimulating the circuit with an RF input, and monitoring its input and output signals at various frequencies and amplitudes.

The advantages of frequency-domain testing versus time domain testing are:

1) standard, programmable instruments can detect and analyze signals. Digital output of relatively few numbers can completely characterize complex waveforms, including distortion, modulation, and spurious responses;
2) bandwidth restrictions of real-time oscilloscopes and the triggering and aliasing problems associated with sampling oscilloscopes are avoided; and
3) large measurement range (>140 dB) facilitates measurements ranging from large-signal switching response to low-level thermal noise.

The disadvantages of this type of frequency domain testing are:

1) phase information can not be readily obtained; and
2) parameters of the time domain (e.g., risetime, delay time) cannot be measured directly.

As a result of these properties, the RF test system is very useful for characterization of RF circuits of all types, but of limited usefulness in characterizing and troubleshooting circuits whose response is essentially time domain. However, adequate tests can be performed on even these switching-type circuits as long as they can be stimulated to deliver a periodic output waveform with a recognizable "Signature". An example of such a test is given later.

The wafer-probing portion of this test system consists of a calculator-controlled automatic wafer stepper and a high-frequency probe card (Fig. 12). DC and RF signals alike are fed to and from the circuit under test on 50-Ω coaxial and microstrip lines. Contact to test wafers is made through a hole drilled in the sapphire probe card via

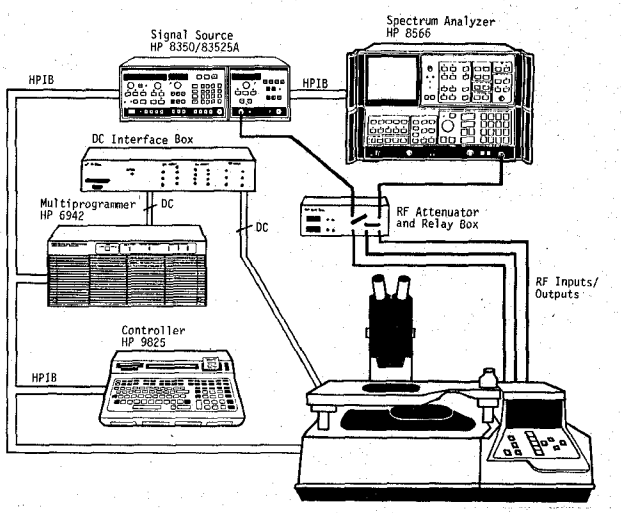


Fig. 10. Diagram of automated RF wafer test system. The calculator controls dc and RF instruments via an IEEE 488 bus. The basis of this system is the programmable spectrum analyzer which can measure linear and nonlinear responses of both digital and analog circuits.

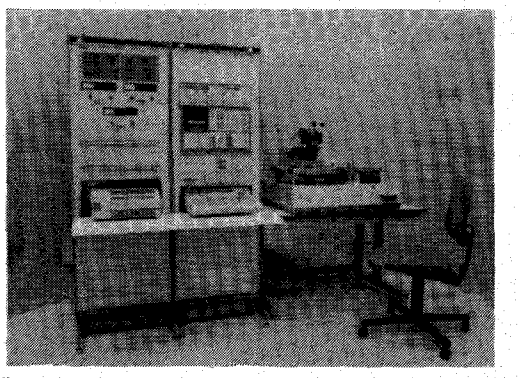


Fig. 11. Photograph of automated RF wafer test system.

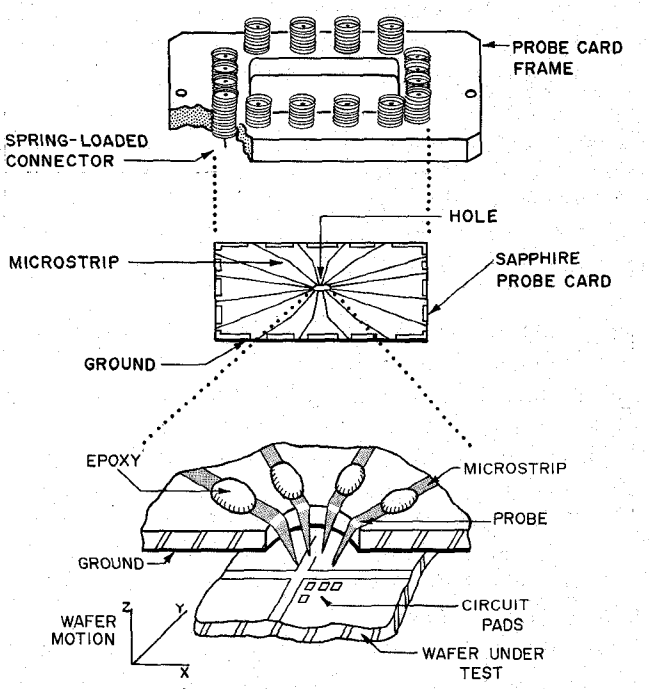


Fig. 12. High-frequency probe card. 50-Ω microstrip lines on a sapphire substrate convey signals to and from the wafer under test via Be–Cu probes protruding through a center hole. The wafer moves, probes are stationary.

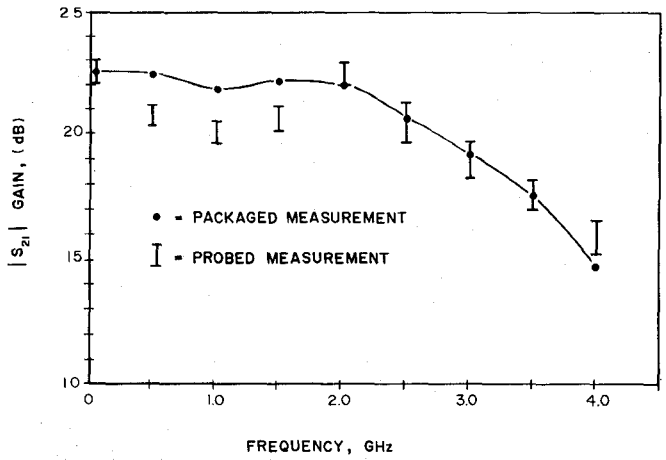


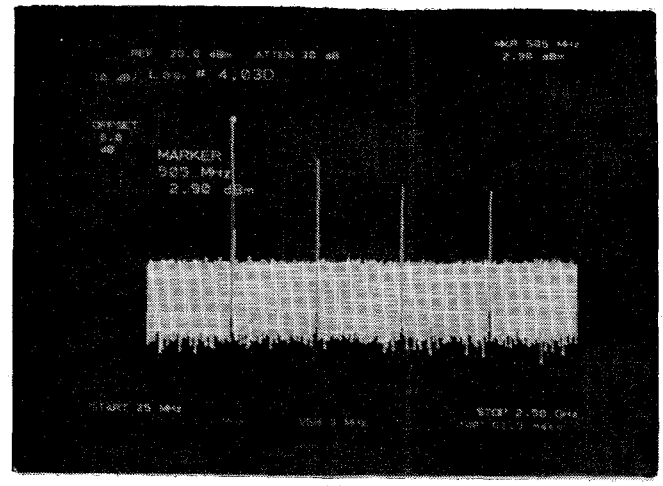
Fig. 13. Amplifier frequency response measurement; packaged and probed. (Bars represent measurement uncertainty).

Be–Cu probes. Where ground is required, a probe is connected to the probe card bottom-side ground plane with a short gold ribbon bond. The probe inductance, 0.7 nH, can present problems, especially in signal ground paths. Also, the 50-Ω characteristic impedance of microstrip lines used as power supply leads can furnish unwanted signal feedback paths. For these reasons, it is often necessary to customize probe card designs (e.g., include power-supply bypass capacitors on the probe card) for particular circuits, and to consider the effects of probe parasitics when laying out chips. Very nearly, however, the same performance that can be obtained from a hybrid-substrate-mounted chip can be observed with the RF wafer probe.

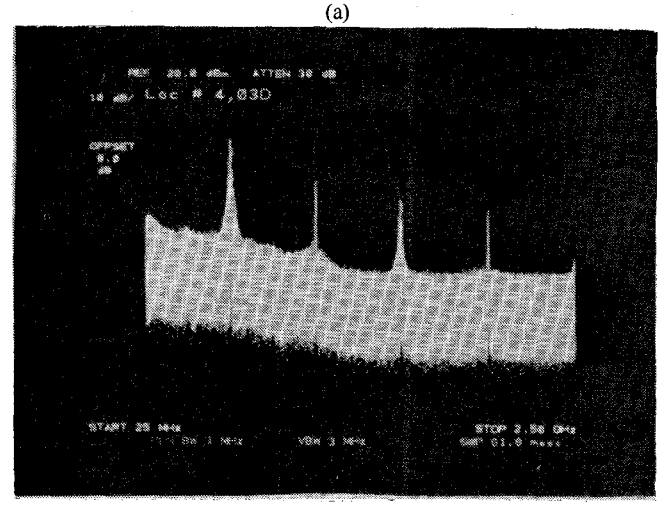
An example of the difference between packaged circuit performance and wafer probe performance of an individual circuit is shown in the frequency response data of Fig. 13. Here, a particular 22-dB gain, 2.5-GHz bandwidth amplifier chip was measured with the probe card and in a microwave package. The measurement uncertainty varies from ±0.5 dB to ±1.0 dB, as indicated by the data bars. At low frequency and high frequency, the packaged performance and probed performance generally agree to within the probe system measurement uncertainty. Corrections for repeatable anomalies, such as the gain "dip" of probed data (0.5–1.5 GHz), can be introduced into the data analysis.

Examples of parameters commonly measured on amplifying circuits are: gain; frequency response; power saturation; harmonic distortion, and noise figure. In production test mode, such circuits can be checked at sufficient predetermined frequencies in 1 min or less. During this test, input bias is optimized, small-signal gain and noise figure are measured at five frequencies, and large-signal gain and distortion checked at five frequencies. The same system is used to perform extended characterization tests which require greater test time.

An example of the frequency domain test response of a circuit normally tested in time domain is shown in Fig. 14. Here, a binary counter, consisting of a master–slave flip-flop, is functionally tested with an input frequency of 1 GHz. Fig. 14(a) shows the signature spectrum expected



(a)



(b)

Fig. 14. Digital circuit frequency domain test example. A binary counter master–slave flip-flop is operating correctly in (a). The easily recognized spectrum displayed in (b) is for marginal, but incorrect, operation.

from a properly functioning unit. Fig. 14(b) shows the response of this circuit with marginal input drive conditions. Often, such marginal operation is difficult to observe on sampling oscilloscopes. In contrast, frequency domain response is easily interpreted, even by an automatic test routine which does not rely on human interpretation. A test of a more complex digital counting circuit, with four different externally controlled modes of operation and a requirement for high-frequency input sensitivity measurement, is performed by this system in less than 3 min. Input bias for best sensitivity is determined, all functional modes tested, and counting sensitivity for nine frequencies is measured.

V. Results

The automated RF test system has been used to collect functional yield data on a variety of circuits, both linear and digital. Data collected for six circuit types from 23 tested wafers is graphed in Fig. 15. Here, four different amplifier circuits (A1–A4) and two digital circuits (D1–D2) have their functional yield percentages (full-wafer, including edges) plotted against active circuit area (devices

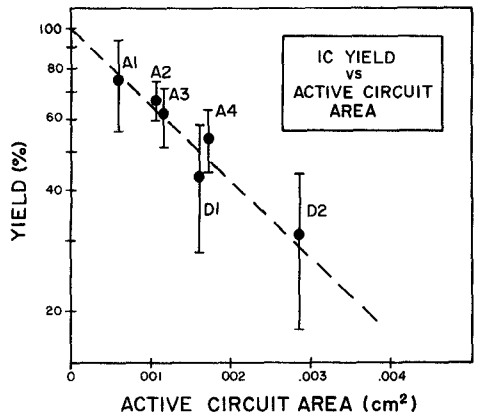


Fig. 15. IC yield for six different circuit designs (A = amplifier type, D = digital type). Average of individual wafer yields is plotted against active circuit area. Bars indicate one standard deviation.

and wiring). Functional yields ranging from 13 percent to 97 percent are included in the data. The inverse relation between yield and active area is evident, with an implied defect density of 440/cm^2 in a homogeneous Poisson distribution [20]. It has been inferred from visual inspection that a high correlation exists between metal-pattern defects of photolithographic origin and circuit defects, but that the majority of these defects are not associated with the 1-μm gate stripes. Therefore, it should not be assumed that this data represents any fundamental limit on GaAs IC technology in general, but rather that it reflects only the experience for the wafer population studied. In fact, the "Window Method" [20] of extrapolating yields was applied to a particularly high-yield wafer of this group. Analysis indicated a uniform Poisson distribution of 100 defects/cm^2, excluding edge defects, rising to a nonuniform density of 240/cm^2 when wafer edges were included. The conclusion drawn is that GaAs IC technology stands to benefit substantially in manufacturing yield by adopting larger wafers and cleaner lithographic procedures. However, present yields (Fig. 15) are wholly adequate for economic manufacturing of small-to-medium-scale GaAs IC's.

VI. Conclusion

We have presented a description of a manufacturing process for GaAs IC's which is intended for a low-volume high variety-of-circuits production environment. Key features include:

1) wafer selection on basis of substrate resistivity;
2) retained anneal cap field oxide for metal lifting assist;
3) proton-damage isolation for reduced backgating and increased isolation breakdown;
4) silicon nitride passivation used as a thin-film capacitor;
5) polyimide intermetal dielectric and scratch protection layers; and
6) on-wafer functional testing and characterization of circuits at microwave frequencies.

Circuit components (FET's, diodes, resistors, capacitors, inductors) were described.

In addition, an automated on-wafer IC tester was described which performs rapid frequency-domain functional tests and circuit characterization measurements at frequencies from 0.1 GHz to >4 GHz.

It is claimed that this manufacturing process offers a practical way to economically produce GaAs IC's in the low-microwave frequency range where we believe they will make substantial contributions to the design and manufacture of electronic instruments and systems.

Acknowledgment

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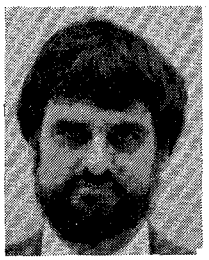

Rory L. Van Tuyl (SM'77) received the B.S. and M.S. degrees in electrical engineering from the University of California, Berkeley, in 1965 and 1969, respectively.

After three years work in nuclear instrumentation at Lawrence Berkeley Laboratory, he joined Hewlett-Packard's Santa Clara Division, Santa Clara, CA, in 1969 to work on high-speed bipolar integrated circuits and microwave frequency counters. From 1973 through 1977 he was principal investigator on the GaAs IC research project at Hewlett-Packard's Solid-State Laboratory. He joined Hewlett-Packard, Santa Rosa, CA, in 1977 to work on GaAs circuit applications and in 1978 became Project Manager for GaAs IC process development and applications.

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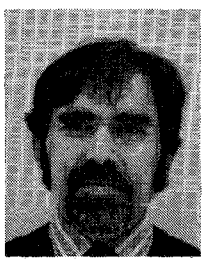

Virender Kumar received his B.S. in Metallurgy from I.I.T. Kanpur, India, in 1965. He received an M.S. in Metallurgy from the University of Minnesota in 1967, and a Ph.D. in materials science from the University of Southern California in 1970, where he studied the defect-structure of II-VI compounds.

He worked at Bell Laboratories, Murray Hill, NJ, from 1970 to 1975 in the area of metallizations, with special emphasis on metal-semiconductor interface reactions. Since joining Hewlett-Packard, Santa Rosa, CA, in 1976, he has worked on GaAs LPE buffer growth, GaAs varactor diode material growth and device processing. He has been involved in GaAs MESFET IC processing for the past three years.

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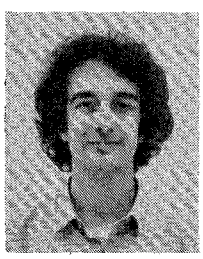

Donald C. D'Avanzo (M'80) received the B.S. degree in biomedical engineering from Brown University, Providence, RI, in 1973, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1974 and 1980, respectively.

His thesis research included characterization and modeling of VMOS and DMOS transistors and spreading resistance measurement development and data analysis. Between March 1977 and August 1979 he worked on a part-time basis at the Integrated Circuit Laboratory of Hewlett-Packard Company, Palo Alto, CA Since March 1979 he has been working at the Santa Rosa Technology Center, Hewlett-Packard Co., Santa Rosa, CA, on process development, characterization, and modeling of GaAs integrated circuits.

Dr. D'Avanzo is a member of Tau Beta Pi, Sigma Xi, and the Electrochemical Society.

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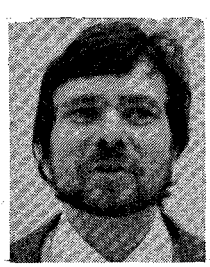
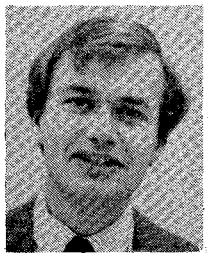


Thomas W. Taylor received the B.S. degree in chemistry from Sonoma State University, Rohnert Park, CA, in 1978.

He joined the Hewlett-Packard Santa Rosa Division in 1978 and worked with GaAs IC process development. He is currently working with GaAs IC process development.



Val E. Peterson (S'73-M'79) received the B.E.E. degree from the University of Minnesota, in 1974, and M.S.E.E. from the University of California, Berkeley, in 1978.

He joined Hewlett-Packard's Santa Rosa division in 1974, where he has worked on production and design of microwave hybrid components. Since 1980 he has contributed to GaAs IC circuit characterization, testing, and test system development.

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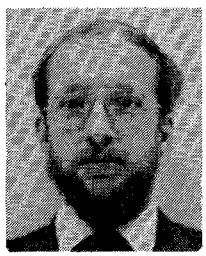

Derry P. Hornbuckle (M'80) received the B.S. degree in engineering from California Institute of Technology, Pasadena, in 1970, and the M.S. degree in electrical engineering from the University of California, Berkeley, in 1976.

From 1968 to 1973 he did audio and RF system design with Executone of Southern California, holding the position of Chief Engineer at the time he left to return to school. At the University of California, Berkeley, from 1973 to 1976, he studied fabrication and microwave applications of Josephson junctions. He has been employed since 1974 as Research and Development Engineer at Hewlett-Packard, Santa Rosa, CA. He has designed microwave amplifiers, oscillators, and components, including a medium-power GaAs MESFET. Since 1977 he has been involved primarily in GaAs monolithic circuit design and has developed and managed automated test facilities for GaAs IC's.

Mr. Hornbuckle is a member of the IEEE Microwave Theory and Techniques and Electron Devices Societies, and a member of the MTT-6 Technical Committee on Microwave and Millimeter-Wave Integrated Circuits.

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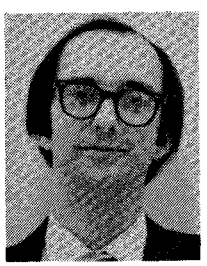

Robert A. Fisher joined Hewlett-Packard in 1970 and has worked in the area of testing GaAs devices since 1974. He has worked with GaAs IC's since 1977; in 1978 he received the AA degree from Santa Rosa Jr. College. He is presently engaged in GaAs IC test system development.

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Donald B. Estreich (M'68) received the B.S.E.E. degree at the University of California, Berkeley, CA, in 1967, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1974 and 1980, respectively. His dissertation was on the physics and modeling of latch-up in CMOS integrated circuits.

From 1967 to 1973 he worked at Teledyne Semiconductor as an R & D Engineer on RF low-noise and RF power bipolar transistors. During 1975 he worked on modeling I^2L at the Santa Clara Division of the Hewlett-Packard Company, and from 1976 to 1978 at the Integrated Circuit Laboratory of Hewlett-Packard Laboratories, Palo Alto, CA, on NMOS integrated circuits. During 1978 he spent six months as a Guest Researcher at Sandia National Laboratories, Albuquerque, NM, investigating CMOS latch-up and radiation effects in MOS integrated circuits. Since May 1979 he has been doing exploratory work on GaAs monolithic integrated circuits at the Santa Rosa Technology Center, Hewlett-Packard Company, Santa Rosa, CA.

During the 1978-1979 academic year Dr. Estreich was a Teaching Fellow at Stanford University. He is also a member of the American Physical Society.